

WHAT IS CLAIMED IS:

1. A system controller in which a plurality of CPUs connected through a shared bus are connected to a plurality of memory units or IO devices through a
5 bus for separate transfer of a read instruction from a read data return, comprising:

holding means for holding a CPU which issues a new instruction and a destination of the instruction, and a CPU which issues an instruction being suspended
10 and a destination of the instruction;

order control means for controlling an issue order of return data and a transfer instruction based on held contents of said holding means in a read time; and

15 issue means for issuing transfers, which are first serialized and transferred through the shared bus, in parallel using a plurality of connection paths.

20 2. The system controller according to claim 1, further comprising

means for queuing a transaction request output to the shared bus after bus snooping through the shared bus.

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3. The system controller according to claim 1, wherein

said order control means comprises
determination means for determining whether or not a
transaction can be issued in response to a read
request based on the held contents of said holding
5 means.

4. The system controller according to claim 3,
wherein

said determination means determines that the
10 transaction cannot be issued when a destination of a
new instruction is IO, and a transfer of an
instruction to a different IO is suspended.

5. The system controller according to claim 3,
15 wherein

said determination means determines that the
transaction cannot be issued when a destination of a
new instruction is memory, and a transfer of an
instruction issued by a different CPU is suspended.

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